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Dated: February 26, 2002 Signature: (Marcus J. Miller)

Docket No.: TESSERA 3.0-102 II DIV (PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Thomas H. DiStefano

Application No.: 09/628,049 Group Art Unit: 2814

Filed: July 27, 2000 Examiner: D. Graybill

For: PACKAGED MICROELECTRONIC ELEMENTS WITH ENHANCED THERMAL CONDUCTION

Commissioner for Patents
Washington, DC 20231

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AMENDMENT

Dear Sir:

In response to the official action mailed August 30, 2001, applicant submits the following amendments and remarks.

IN THE CLAIMS

CLEAN COPY OF AMENDED CLAIMS:

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9. (AMENDED) A method of enhancing the reliability of electrical connections in a semiconductor package during operation of the chip, comprising the steps of:

(a) providing a semiconductor chip having a front surface and a rear surface, said front surface having contacts;

(b) providing flexible leads extending from said contacts on said front surface of said chip by wire bonding, said flexible leads being connected to said contacts at joints on said front surface;

(c) placing a spreader above said front surface, said spreader having a coefficient of thermal expansion

substantially equal to the coefficient of thermal expansion of said chip; and

(d) disposing a liquid encapsulant between said front surface and said spreader and around said leads and curing said encapsulant, whereby the motion of the leads during thermal cycling is constrained.

10. (AMENDED) The method as claimed in claim 9, further comprising the step of providing a predetermined geometry for the cured encapsulant so as to affect the constraint of the leads.

Insert new claims 11-17, as follows:

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11. (NEW) A method as claimed in claim 9 wherein said steps of placing said spreader and disposing and curing said encapsulant are performed so that the cured encapsulant has edges intersecting said spreader and extending downwardly away from said spreader and said spreader extends outwardly beyond intersections of said edges and said spreader.

12. (NEW) A method as claimed in claim 11 wherein said steps of placing said spreader and disposing and curing said encapsulant are performed so that said edges of said cured encapsulant include opposite edges sloping outwardly away from one another in the downward direction away from said spreader.

13. (NEW) A method as claimed in claim 9 wherein said step of providing said flexible leads by wire bonding includes forming bonding wire so that said bonding wire includes loops projecting upwardly away from said front surface and away from said joints.

14. (NEW) A method as claimed in claim 13 wherein said step of forming bonding wire includes forming downwardly-projecting portions extending from said loops downwardly beyond the front surface of the chip.

15. (NEW) A method of making a semiconductor package comprising the steps of:

(a) positioning a semiconductor chip having a front surface with contacts thereon and having a rear surface and an element having conductive features thereon so that said element extends beneath said rear surface of said chip and said front surface of said chip faces upwardly away from said element;

(b) providing flexible leads extending from said contacts on said front surface of said chip and extending downwardly to said element, said flexible leads being connected to said contacts at joints on said front surface;

(c) placing a spreader above said front surface, said spreader having a coefficient of thermal expansion substantially equal to the coefficient of thermal expansion of said chip; and

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(d) disposing a liquid encapsulant between said front surface and said spreader and around said leads and curing said encapsulant, whereby the motion of the leads during thermal cycling is constrained.

16. (NEW) A method as claimed in claim 15 wherein said step of providing said flexible leads is performed by wire bonding.

17. (NEW) A method as claimed in claim 16 wherein said step of wire bonding includes forming bonding wire into loops projecting upwardly from said front surface and downwardly-projecting portions extending downwardly from said loops to said element.